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(54) Parallel multi-phased amorphous silicon shift register for fast addressing of an amorphous silicon array.

(57) A shift register assembly having an integrated multi-phased dynamic shift register (50) with a corresponding multi-phased driving buffer (60) for addressing elements of an array. The shift register and buffer combination is used to select segments on the array having a common select line (V_{ϕ}) thus reducing the number of input lines needed to address such an array. Furthermore, the multi-phased operation of the shift register allows for faster operation than that of a traditional shift register setup.

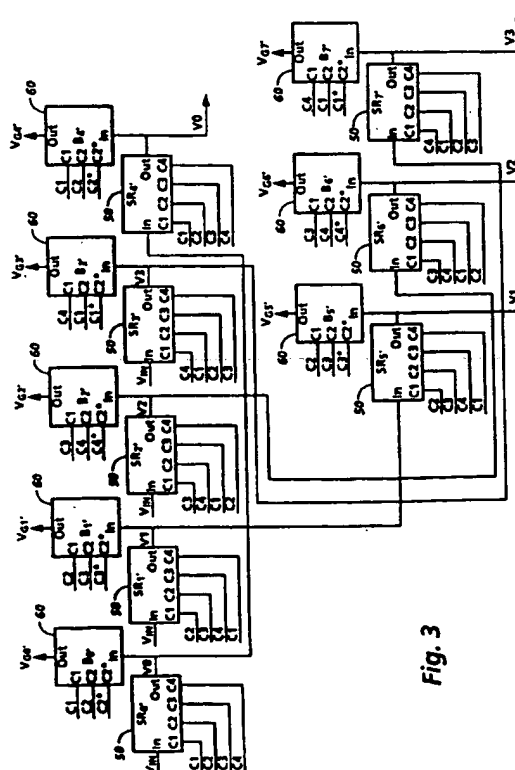


Fig. 3

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EUROPEAN SEARCH REPORT

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EP 93 30 3040

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. CL.5)
P,X Y A	US-A-5 136 622 (PLUS) * column 1, line 29 - line 44 * * column 2, line 1 - line 36 * * column 3, line 10 - line 11; figures 1,2 * ---	1,2,4 7 3,5,6	G11C8/04
D,Y	US-A-4 466 020 (O'CONNELL) * abstract * * column 2, line 51 - line 58 * ---	7	
X	EP-A-0 342 925 (SEIKO EPSON CORPORATION) * page 1, line 36 - line 42 * * page 1, line 52 - line 58 * * page 2, line 11 - line 22; figures 13A, 13B * -----	1,2,4	
			TECHNICAL FIELDS SEARCHED (Int. CL.5)
			G11C
The present search report has been drawn up for all claims			
Place of search THE HAGUE		Date of completion of the search 14 June 1995	Examiner Gonzalez Ordonez, O
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